COLLEGE OF ENGINEERING
MECHANICAL AND ELECTRICAL DEPARTMENT

Course Name: DIGITAL SYSTEMS DESIGN
Course ID:
Faculty Curse ID: 5673
University Course ID: **CACEI ID:** CI
Study plan level: VI; IMT, IEA **Credits:** 7
Normal hours per week: 3 **Total hours course:** 48
Lab hours per week: 1
Complementary Practices:
Extra-class Work Hours / Week: 3
Course type: IME, IEA, IMT/ Mandatory own area
Approved credits needed:
Curricular last revision date: 2013

Prerequisite course ELECTRONICS I (5590)

COURSE JUSTIFICATION

In the Mechatronics Engineering and Automation areas the use of digital systems based on combinational and sequential blocks are of great importance to solve control problems by using digital tools. This course is designed for students to know and understand the basic principles of combinational and sequential logic circuits, and the design of digital high-speed systems based on hardware description languages such as VHDL and its implementation in FPGA and PLD systems.

COURSE OBJECTIVE

The course objective is to present, as clearly as possible the principles of logical systems. Enter the basic principles and ideas, which are used in all digital systems such as Boolean algebra, both combinational and sequential logic. Familiar with VHDL hardware description language concepts.

COURSE TOPICS

1. Introduction to Logic Circuits

7 hrs.

Objective: Presenting the basics of digital electronics and learn the available tools for designing digital circuits using HDL hardware description languages.

1.1.- Variables and functions
1.2.- Inversion
1.3.- Truth tables
1.4.- Logic gates and networks
1.5.- Boolean algebra
1.6.- Synthesis using AND, OR and NOT gates
1.7.- NAND and NOR logic networks
1.8.- Introduction to CAD tools
1.9.- Introduction to descriptive languages
1.10.- Implementation technology

2. Optimized implementation of logic functions

7 hrs.

Objective: Learn synthesis tools to minimize combinational logic functions.

2.1.- Karnaugh map
2.2.- Strategy for minimization
2.3.- Minimization of product-of-sums forms
2.5.- Incompletely specified functions
2.5.- Multiple-output circuits
2.6.- A tabular method for minimization
2.7.- Circuits synthesized from VHDL

3. Number representation and arithmetic circuits

5 hrs.

Objective: Learn the different numerical representations and understand algorithms for basic arithmetic operations.

3.1.- Positional number representation
3.2.- Addition of unsigned numbers
3.3.- Signed numbers
3.4.- Fast adders
3.5.- Design of arithmetic circuits using CAD tools
3.6.- Multiplication
3.7.- Booth-Radix algorithms for multiplication
3.8.- Other number representations

4. Combinational-circuit building blocks

8 hrs.

Objective: Combinational digital circuit design using VHDL.

4.1.- Multiplexers
4.2.- Decoders
4.3.- Encoders
4.4.- Code converters
4.5.- Arithmetic comparison circuits
4.6.- VHDL for combinational circuits

5. Memory circuits

6 hrs.

Objective: Enter sequential logic principles, operation of flip - flop.

5.1.- Basic latch.
5.2.- Gated SR latch
5.3.- Gated D latch
5.4.- Master-slave and edge-triggered D flip-flops
5.5.- T flip-flop
5.6.- JK flip-flop
5.7.- Registers
5.8.- Counters
5.9.- Memory circuit design with VHDL

6. Synchronous sequential circuits

6 hrs.

Objective: Designing finite state machines using flip-flops and their implementation in registers, counters and other applications.

6.1.- Design Strategy
6.2.- State Assignment
6.3.- Mealy topology
6.4.- Moore topology
6.5.- Design of finite state machines with CAD tools

7. Digital system design

9 hrs.

Objective: Apply acquired tools to design complex digital systems and understand the foundation of a basic processor.

7.1.- Building block circuits
7.2.- Shift registers
7.3.- Memories
7.4.- Rationale for processor design

METHODOLOGY

Theoretical concepts are presented and subsequently application exercises. Must perform tasks or theoretical projects, simulation or implementation.

EVALUATION CRITERIA

5 partial assessments are performed with a maximum duration of 1 hour. These tests represent 80% of the partial qualification. Tasks and / or projects to be delivered on the due date will be assigned, they will be worth 20% of the partial qualification. To pass the course, students must prove the corresponding laboratory. No final grade will be given until we have laboratory skills

BIBLIOGRAPHY

TEXT BOOK:

Mandatory

1. Stephen Brown, Zvonko Vranesic, Fundamentos de Lógica Digital con Diseño VHDL, McGraw Hill, 2ª Edición, 2005.

Further

2. M. Morris Mano, Diseño Lógico, Pearson/Prentice Hall, 3ª Edición, 2003.

3. M. Morris Mano, Charles R. Kime, Fundamentos de Diseño Lógico y Computadoras, Pearson/Prentice Hall, 3ª Edición, 2005.
4. IEEE Std 1076-2008 (Revision of IEEE Std 1076-2002) "IEEE Standard VHDL Language Reference Manual, 2009.